REMARKS

Claims 1-20 are pending in the application. Claims 1-8, 10, 16, 19, and 20 stand rejected. Applicants gratefully acknowledge the Examiner's indication that claims 9, 11-15, 17 and 18 include allowable subject matter and would be allowable if rewritten as indicated. The Examiner's reconsideration of the claim rejections is respectfully requested in view of the above amendment and the following remarks.

Claim Rejections - § 103(a)

(1) Claims 1-3, 5, 10, 16 and 19-20 are rejected as being unpatentable over Applicant's admitted prior art FIG. 1 (hereafter, "APA") in view of Shirota (U.S. Patent Application Publication 2003/0142773), as set forth on pages 2-4 of the Final Action.

Applicants respectfully submit that at the very minimum, the combination of APA and Shirota is legally deficient to establish a *prima facie* case of obviousness against claims 1, 16, and 20.

Claim 1 has been amended to recite, *inter alia*, "*each of the first and second clock signal groups comprises at least two different inputted clock signals having different phases from each other*". Claims 16 and 20 have been amended in a similar manner. For example, amended claim 16 recites, *inter alia*, "*each of the first and second clock signal groups comprising at least two different inputted sampling clock signals, wherein each sampling clock signal has a unique phase*", and amended claim 20 recites, "*each set of OSR sampling clock signals comprise at least two different inputted clock signals* having different phases from each other".

The Examiner continues to maintain that element 11 (PLL) of APA teaches a clock signal generating circuit that generates at least two clock signal groups. The Examiner interprets each single clock signal generated by the PLL as being a single clock

signal group. This interpretation contradicts the language of amended claim 1, which describes each clock signal group as comprising "*at least two different inputted clock signals having different phases from each other*". Since the claimed clock signal generating unit generates at least two clock signal groups, each having *at least two different inputted clock signals having different phases from each other",* the claimed clock signal generating unit generates at least 4 clock signals. However, the PLL only generates 3 clocks signals, namely CLKA, CLKB, and CLKC. Thus, the APA does not teach the claimed clock signal generating circuit.

Further, the deficiencies of APA in this regard are not cured by Shirota. For example, Shirota merely teaches (in para. 0035 and FIG. 2) a data recovery circuit receiving a single clock signal group 109. However, a second clock signal group is not taught.

Applicants had previously argued that the combination of APA and Shirota does not disclose or suggest "*oversampling the serial data by using a dynamically selected one of the at least two clock signal groups"*, as recited in claim 1.

The Examiner acknowledges (in p.3 of the Office Action dated March 20, 2007) that the APA fails to teach *oversampling the serial data by using a dynamically selected one of the at least two clock signal groups*, but contends that such a limitation is taught by element 104 (DCR circuit) and paragraph 0035 of Shirota.

However, Shirota merely teaches selecting a single clock signal from a single clock signal group 109. For example, paragraph 0035 of Shirota states that "the DCR circuit 104 selects from the clock signal group 109 the optimum clock signal for loading the receive output". The teaching in Shirota of selecting a single clock signal from a

single clock single group does not teach using a dynamically selected one of at least two clock signal groups.

It was also previously argued that the combination of APA and Shirota does not disclose or suggest *the selection depending upon the number of edges of clock signals of the selected one of two clock signal groups being within an eye open region of the serial data*, as recited in claim 1.

The Examiner continues to rely on the DCR circuit 104 and paragraphs 0011 and 0035 of Shirota as disclosing *the selection depending upon the number of edges of clock signals of the selected one of two clock signal groups being within an eye open region of the serial data.*

However, the DCR circuit 104 of Shirota merely (in paragraph 0035) compares the phase of a receiver output signal with phases of clock signals of a single clock signal group to select an optimum signal, and not to select a clock signal group.

Further, the claimed selection generally depends on frequency, whereas the selection performed in Shirota depends on phase. The number of edges of a signal within a region yields information about the frequency of that signal within that region, and not the phase. For example, a first signal that has more edges in a region than a second signal would have a higher frequency in that region.

For at least the foregoing reasons, claim 1 is believed to be patentable over the combination of APA and Shirota. Claims 2-3, 5, and 10 are believed to be patentable over said combination at least by virtue of their dependence from claim 1.

Claim 16 is believed to be patentable over the combination of APA and Shirota for at least similar reasons to claim 1. For example, said combination does not disclose or suggest, e.g., "*each of the first and second clock signal groups comprising at least two*

different inputted sampling clock signals" and "*a data recovery circuit that recovers the effective data from the serial data by sampling the serial data by the sampling clock signals of a dynamically selected one of the at least two sampling clock signal groups*", as recited in claim 16. Claim 19 is believed to be patentable over said combination at least by virtue of its dependence from claim 16.

Claim 20 is believed to be patentable over the combination of APA and Shirota for at least similar reasons to claim 1. For example, said combination does not disclose or suggest, e.g., "*each set of OSR sampling clock signals comprise at least two different inputted clock signals having different phases from each other*" and "*the selected set of OSR sampling clock signals has been dynamically selected so as to sample the serial data by a plurality of sampling clock signals having edges within the eye open region of the serial data*", as recited in claim 20.

(2) Claims 4 and 6 are rejected as being unpatentable over APA, Shorota, and U.S. Patent 6,807,233 to Sato, **(3)** Claim 7 is rejected as being unpatentable over APA, Shirota and U.S. Patent 5,528,198 to Baba, and **(4)** Claim 8 is rejected as being unpatentable over APA, Shirota and U.S. Patent 7,103,343 to Boss.

The above obviousness rejections (2~4) are legally deficient as a matter of law at least to the extent that the rejections are premised on the combination of APA and Shirota, at least for the reasons stated above for the base claim 1, from which claims 4, 6, 7, and 8 depend.

Withdrawal of the claim rejections under 35 U.S.C. § 103 is respectfully requested.

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

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